## IN THE CLAIMS:

## **CLAIMS**

## What is claimed is:

- (Currently Amended) A method of forming a package device (10, 100), comprising; providing a package substrate (12) having a first side (50, 150) and a second side (52, 152) and having first pads (16, 116) on the first side and second pads (16, 116) on the second side;
  - placing a first integrated circuit (22, 122) on the first side and a second integrated circuit (32, 132) on a second side;
  - electrically connecting the first integrated circuit to the first pads and the second integrated circuit to the second pads; and
  - testing the first integrated circuit and the second integrated circuit by applying test probes (44, 144) to the first pads and the second pads.
- 2. (Currently Amended) A method for forming a package device (10, 100), comprising: providing a package substrate (12, 112) having a first surface (50, 150) along a first plane and second surface (52, 152) along a second plane, wherein the package substrate has a cavity (20, 120) between the first plane and the second plane; placing a first integrated circuit (22, 122) in the cavity;
  - placing a second integrated circuit (32, 132) adjacent to the first integrated circuit outside the cavity; and
  - depositing encapsulating material (28, 46, 138, 146) over the first integrated circuit and the second integrated circuit.
- 3. (Currently Amended) The method of claim 2, wherein the step of depositing comprises: depositing a first portion (28, 128) of the encapsulating material over the first integrated circuit (22, 122) prior to the step of placing the second integrated circuit; and depositing a second portion (46, 146) of the encapsulating material over the second integrated circuit (32, 132).

- 4. (Currently Amended) The method of claim 2, wherein the package substrate (12, 112) further comprises a supporting member (18, 119) along the second plane (52, 152) of the substrate.
- 5. (Currently Amended) The method of claim 4, further comprising removing the supporting member (18, 119) prior to step of placing the second integrated circuit (32, 132).
- 6. (Currently Amended) A package device (10, 100), comprising:
  - a package substrate (12, 112) having a first surface (50, 150) defining a first plane and a second surface (52, 152) defining a second plane, the package substrate having a cavity (20, 120) between the first plane and the second plane;
  - a first integrated circuit (22, 122) in the cavity; and
  - a second integrated circuit (32, 132), coupled to the package substrate, outside the cavity.
- 7. (Currently Amended) A package device (10, 100), comprising:
  - a package substrate (12, 112) having a first side and a second side;

first pads (16, 116) on the first side;

second pads (16, 116) on the second side;

- a first integrated circuit (22, 122) mounted to the package substrate;
- wherein the first pads and the second pads are further characterized as being useful for receiving test probes (44, 144) for testing.
- 8. (Currently Amended) The package device of claim 7, further comprising a second integrated circuit (32, 132) mounted to the package substrate.
- 9. (Currently Amended) The package device of claim 8, wherein:

the first integrated circuit (22, 122) is electrically connected to the first pads (16, 116); and

- the second integrated circuit (32, 132) is electrically connected to the second pads (16, 116).
- 10. (Currently Amended) The package device of claim 9, wherein the substrate (12, 112) is further characterized as having a cavity (20, 120) and the first integrated circuit (22, 122) is further characterized as being in the cavity.